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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/681,856	**Applicant(s)** CHAI ET AL.
	Examiner Mujtaba K. Chaudry	**Art Unit** 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 August 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,4,7,12-14 and 20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4,7,12-14 and 20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 12, 2005 has been entered.

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1, 4, 7, 12-14 and 20 filed August 12, 2005 have been fully considered but are not persuasive.

Applicant contends, "...the prior arts of record do not teach or suggest a plurality of memory arrays, each memory array comprising a compilable address magnitude comparator..." The Examiner respectfully disagrees. Adams teaches (Figure 5 and associated text) a plurality of memory arrays, each memory array comprising a compilable address magnitude comparator. The Examiner would like to point out, with regards to Applicants arguments that the CAM is located external to the memories, that Adams teaches a BIST, which shows that the CAMs to be internal as can be seen in Figure 5 as well. See Figure 5:

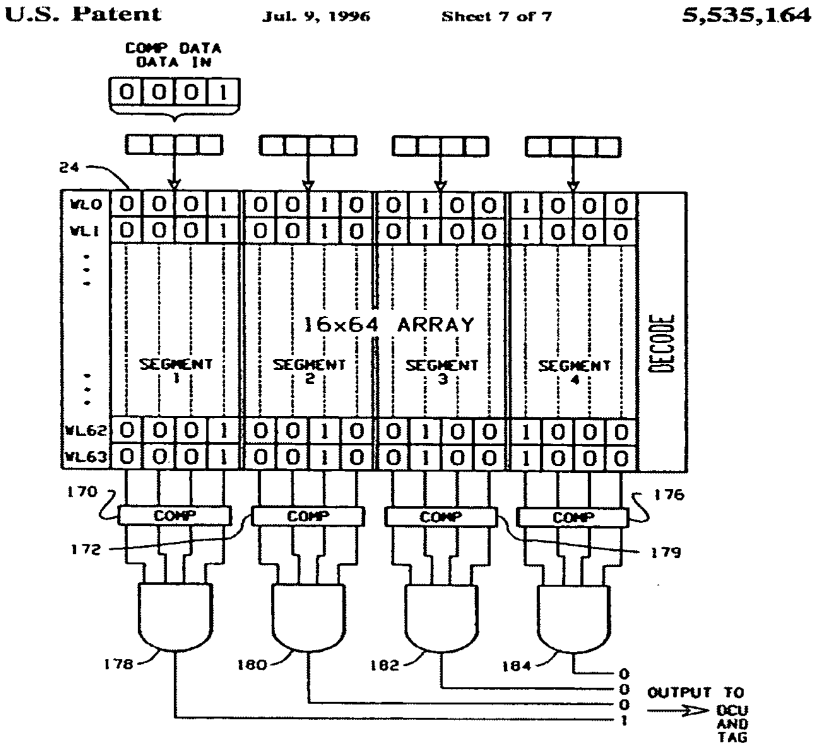

FIG. 5

Applicants contend, "...the prior arts of record do not teach a compilable address magnitude comparator..." The Examiner respectfully disagrees and would like to point out that by definition the term "compilable" is derived from the root word "compile" which is defined as, *"to translate a computer program expressed in a high-order language into its machine language"*. In other words, it is a translation perform by a computer program which is necessarily included with the testing process of Adams, and in general any memory testing procedure. Applicants are also reminded that although the Applicants are entitled to be their own lexicographers, they are not entitled to give a term a meaning other than the one that is commonly known in the art and is defined by a standard. See MPEP 2111.

Applicants contend, "...the prior arts of record do not teach or suggest the compilable address comparator to override the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory…" Adams teaches (cols. 14-15) test memory 24, test patterns supplied by BIST are first written into the four 4-bit segments per wordline in the illustrative 64.times.16 bit CAM of FIG. 5, and then the data to be compared is applied to the compare data inputs and the comparison made to see if the data originally written compares with the compare data. This comparison is done by means of four comparators 170,172,174,176, the comparator 170 being configured to compare the data in the first 4-bit segment on a wordline, comparator 172 being configured to compare the data in the second 4-bit segment, comparator 174 being adapted to compare the data of the third 4-bit segment, and comparator 176 being configured to compare the four bits of data in the fourth 4-bit segment on a wordline. Each comparator block (170, 172, 174, and 178) is comprised of four 2-input XNOR gates. The output of comparator 170 provides the inputs to an AND gate 178, comparator 172 provides the inputs to AND gate 180, comparator 174 provides the input to AND gate 182, and comparator 176 provides the inputs to AND gate 184. The output of the AND gates 178, 180, 182,184 are then outputted to the DCU memory 12 and TAG memory 14. If the comparison between a 4-bit segment and the compare data is true, then its respective 4-bit segment comparator logic block will output four "1"s to the AND gate it feeds, which in turn will output a "1" indicating a successful comparison between that segment and the compare data. If, however, there is a difference between one or more of the bits in the stored segment pattern and the compare data, then its respective segment comparator logic will not output all "1"s and the AND gate it feeds will output a "0" indicating a mis-compare between that segment and the compare data. For instance, if at the currently selected wordline, segment 1 contains the bit pattern 0001 while segments 2-4 contain 0010, 0100, and 1000, respectively, and the 4-bit compare data pattern presented to the CAM 24 input is 0001, then segment 1 comparator block 170 will output four "1"s, causing AND gate 178 to output a "1". Since the compare data pattern does not match the patterns stored in segments 2-4, comparator logic 172, 174 and 176 will not output all "1"s causing the AND gates they feed 180, 182, 184, respectively, to output "0"s. The output of the CAM in this example will therefore be 1000.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1, 4, 7, 12-14 and 20. All arguments have been considered. It is the Examiner's conclusion that amended claims 1, 4, 7, 12-14 and 20 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4, 7, 12-14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. (USPN 5535164) further in view of AAPA.

As per claims 1, 7 and 12, Adams et al. (herein after: Adams) substantially teaches (title and abstract) a single BIST which can test various memories of different sizes, types and characteristics by using a state machine to select and generate all patterns required for testing all of the memories on the chip, and impressing all of the data, including expected data, and address information on all of the memories simultaneously. The BIST also generates unique (separate) control signals for the various memories and impresses these control signals on the various memories. The BIST selectively asserts the various control signals so as to apply (write) the data and to read and capture (load result) failure information only to/from those memories whose unique controls are asserted. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write and leakage defects while selective assertion of a memory's load result signal is performed only when valid memory output data is expected so as not to capture false error information. The control signals instruct those memories that do not use a particular sequence of inputs or any portion of a given sequence of inputs to "ignore" such signals, thereby generating the necessary signals to form the test patterns for each and every memory, the data and address information for those patterns, the control signals to write and read each memory, and capture error information for that particular memory. A single BIST can be used to test a multiplicity of memories of different sizes and different types. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write defects and cell leakage defects. Selective assertion of a memory's load result signal prevents capture of a false fail signal due to potentially inverted data stored in the memory in the second and subsequent address accesses. Adams teaches (col. 3, lines 20-56) the BIST circuit 10 shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern. Rewriting a memory can potentially mask charge leakage problems in the cells. When the maximum address is reached, the state machine enters a WAIT state, resets the address counter, and performs various updates, including the assertion of a new subcycle. Furthermore, Adams teaches (col. 4, line 57—col. 5, lines 1-16) a content addressable memory (CAM) 24. The memory 24 is a 512 X 10 bit memory, with the 512 entries broken up into groups of eight 10-bit comparators. A content addressable memory (CAM) is one in which binary data written therein is stored at the various address locations, but in this embodiment said stored data cannot be directly read out. The Cam memory performs the function of comparing binary data asserted thereon to determine if it has a particular bit pattern stored therein. If a pattern is so stored, the CAM memory responds by outputting an appropriate output signal, e.g., a binary "1", and if the pattern is not stored, a binary "0", on the output of each comparator depending on the data stored. Expressed another way, the CAM memory 24 acts as a comparator in which bits are stored in pre-selected patterns which correspond to portions of an address for another memory, and when a bit pattern is impressed on the CAM 24, the CAM 24 compares the impressed bit pattern with the stored bit patterns to determine if the particular bit pattern is stored, and which one of eight comparators found the bit pattern. Thus, the test function of the CAM requires an inputting of various test data and then performing a compare function between data stored therein and binary test data impressed thereon and determining if the output response is appropriate to indicate such a stored data being present at a given location or not.

Adams does not explicitly teach the address comparator to be a "compilable address magnitude comparator" as stated in the present application.

However, the specification on the present application teaches (specification, pages 1-4), in part, the compilable magnitude comparator address comparator overrides the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory. The Examiner would like to point that Adams teaches, as previously stated, a single BIST which can test various memories of different sizes, types and characteristics, wherein the BIST shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Adams by incorporating a "compilable address magnitude comparator" within the method and apparatus. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by making the address magnitude compilable would enable it to efficiently override the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory.

As per claims 13 and 14, Adams substantially teaches, in view of above rejections, (cols. 11-13) comparing the rows and columns against maximum thresholds. The Examiner would like to point out the functionality if the row and column comparator is inherently included since both rows and columns are compared.

As per claim 4, Adams substantially teaches, in view of above rejections, a single BIST which can test various memories of different sizes, types and characteristics, wherein the BIST shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern.

As per claim 20, Adams substantially teaches, in view of above rejections, a single BIST which can test various memories of different sizes, types and characteristics by using a state machine to select and generate all patterns required for testing all of the memories on the chip, and impressing all of the data, including expected data, and address information on all of the memories. The BIST selectively asserts the various control signals so as to apply (write) the data and to read and capture (load result) failure information only to/from those memories whose unique controls are asserted. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write and leakage defects while selective assertion of a memory's load result signal is performed only when valid memory output data is expected so as not to capture false error information. The control signals instruct those memories that do not use a particular sequence of inputs or any portion of a given sequence of inputs to "ignore" such signals, thereby generating the necessary signals to form the test patterns for each and every memory, the data and address information for those patterns, the control signals to write and read each memory, and capture error information for that particular memory. A single BIST can be used to test a multiplicity of memories of different sizes and different types. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write defects and cell leakage defects. Selective assertion of a memory's load result signal prevents capture of a false fail signal due to potentially inverted data stored in the memory in the second and subsequent address accesses.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
September 9, 2005

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